# MT4902

## P-Channel Enhancement Mode Field Effect Transistor

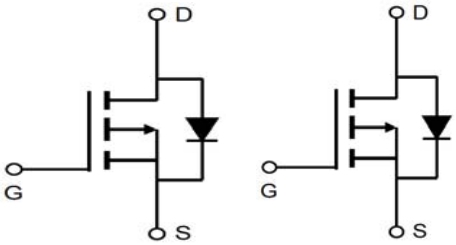
MT Semiconductor®

http://www.mtsemi.com

### Product Summary

| PRODUCT SUMMARY | | |
|---|---|---|
| $V_{DSS}$ | $I_D$ | $R_{DS(ON)}$ (mΩ) Typ |
| -20V | -2.6A | 88@ $V_{GS}$=-4.5V |
| | | 120@$V_{GS}$=-2.5V |

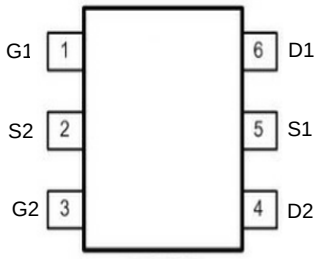
### Simplified Schematic




### Features

- Super high dense cell design for low $R_{DS(ON)}$
- Rugged and reliable
- Simple drive requirement
- Sot-23-6 package

### MARKING DIAGRAM & PIN ASSIGNMENT




SOT-23-6

### Applications

- Portable battery packs
- Load switch

## Absolute Maximum Ratings ($T_A$=25℃unless otherwise noted)

| Parameter | Symbol | Limit | Unit |
|---|---|---|---|
| Drain-Source Voltage | $V_{DS}$ | -20 | V |
| Gate-Source Voltage | $V_{GS}$ | ±10 | V |
| Drain Current-Continuous | $I_D$ | -2.6 | A |
| Drain Current-Pulsed (Note 1) | $I_{DM}$ | -13 | A |
| Maximum Power Dissipation | $P_D$ | 1.0 | W |
| Operating Junction and Storage Temperature Range | $T_J$,$T_{STG}$ | -55 To 150 | ℃ |

## Thermal Characteristic

| | | | |
|---|---|---|---|
| Thermal Resistance,Junction-to-Ambient (Note 2) | $R_{\theta JA}$ | 125 | ℃/W |

## Electrical Characteristics ($T_A$=25°C, unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **● Static Characteristics** | | | | | | |
| $BV_{DSS}$ | Drain-Source Breakdown Voltage | $V_{GS}$= 0V, $I_D$= -250μA | -20 | - | - | V |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = -250μA | -0.4 | -0.7 | -1.0 | V |
| $I_{GSS}$ | Gate-Body Leakage Current | $V_{GS}$=±10V,$V_{DS}$=0V | - | - | ±10 | nA |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = -20V, $V_{GS}$ = 0V | - | - | -1 | μA |
| | | $V_{DS}$ = -20V, $V_{GS}$ = 0V, $T_J$ = 85℃ | - | - | -30 | |
| $R_{DS(on)}$ | Drain Source On State Resistance [3] | $V_{GS}$=-4.5V, $I_D$=-2A | - | 88 | 120 | mΩ |
| | | $V_{GS}$=-2.5V, $I_D$=-1A | - | 120 | 150 | |
| $g_{fs}$ | Forward Transconductance[3] | $V_{DS}$=-5V,$I_D$=-2A | 5 | - | - | S |
| $V_{SD}$ | Diode Forward Voltage[3] | $V_{GS}$ = 0V, $I_S$ = -2.6A | - | -0.8 | -1.2 | V |
| **● Dynamic Characteristics[4]** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$= -10V, $V_{GS}$=0V, f=1MHz | - | 325 | - | pF |
| $C_{oss}$ | Output Capacitance | | - | 63 | - | |
| $C_{rss}$ | Reverse Transfer Capacitance | | - | 37 | - | |
| $Q_g$ | Total Gate Charge | $V_{DS}$ = -10V, $V_{GS}$ = -4.5V, $I_D$ = -2A | - | 3.2 | - | nC |
| $Q_{gs}$ | Gate-Source Charge | | - | 0.6 | - | |
| $Q_{gd}$ | Gate-Drain Charge | | - | 0.9 | - | |
| $t_{d(on)}$ | Turn-On Delay Time | $V_{DD}$ = -10V, $R_L$ = 1.5Ω<br>$I_D$= -1.0A, $V_{GEN}$ = -10V, $R_G$ = 3Ω | - | 11 | - | nSec |
| $t_r$ | Rise Time | | - | 5.5 | - | |
| $T_{d(off)}$ | Turn-Off Delay Time | | - | 22 | - | |
| $t_f$ | Fall Time | | - | 8 | - | |
| $R_g$ | Gate Resistance | $V_{GS}$=0, $V_{DS}$=0, f=1MHz | - | 3 | - | Ω |
| $t_{rr}$ | Body Diode Reverse Recovery Time | $I_F$ = -2A, di/dt = 100A/μs | - | 25 | - | nSec |
| $Q_{rr}$ | Body Diode Reverse Recovery Charge | | - | 10 | - | nC |

## Notes:

**1.** Repetitive Rating: Pulse width limited by maximum junction temperature.
**2.** Surface Mounted on FR4 Board, t ≤ 10 sec.
**3.** Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
**4.** Guaranteed by design, not subject to production

## Typical Electrical and Thermal Characteristics

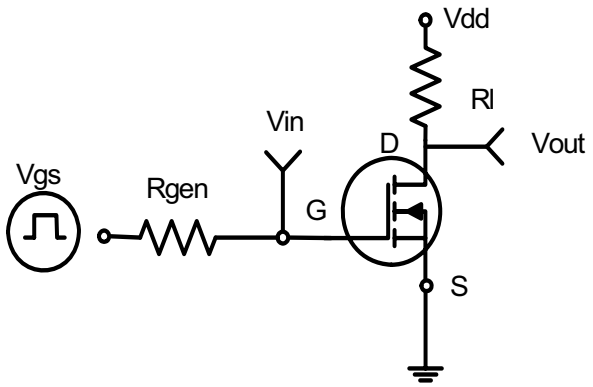



**Figure 1:Switching Test Circuit**

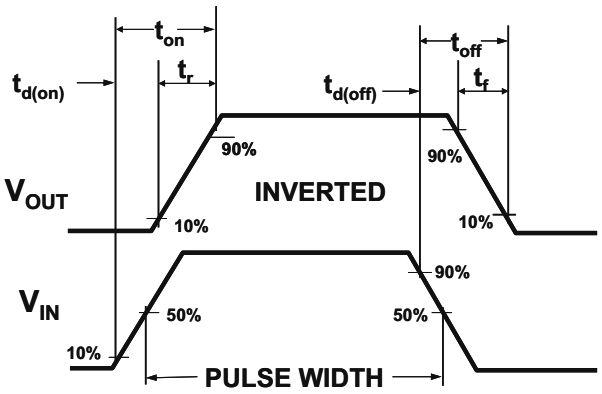



**Figure 2:Switching Waveforms**

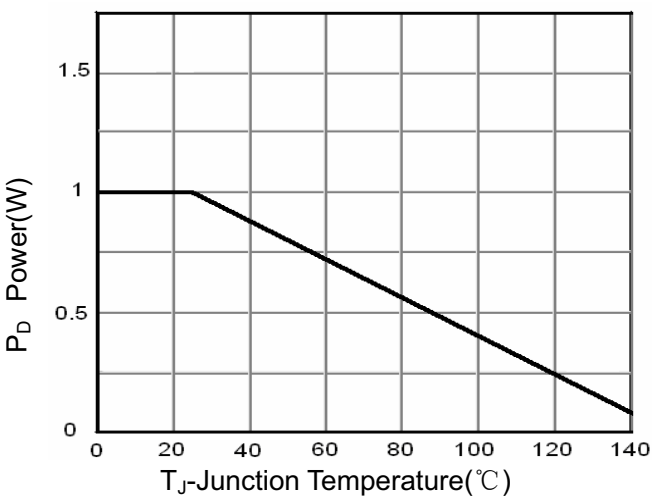



**Figure 3 Power Dissipation**

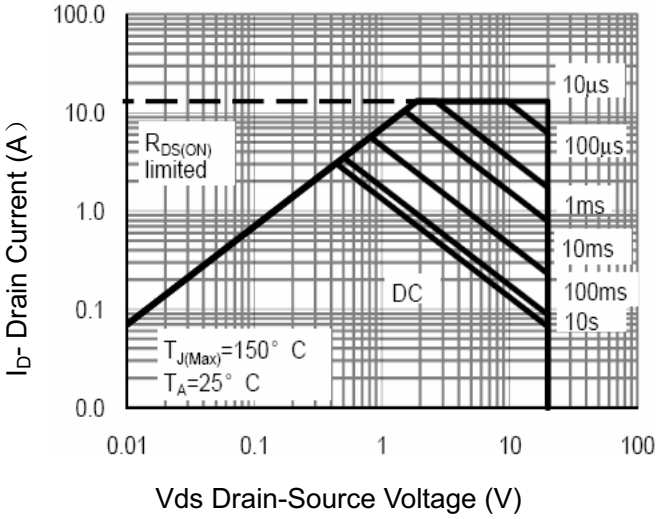



**Figure 4 Safe Operation Area**

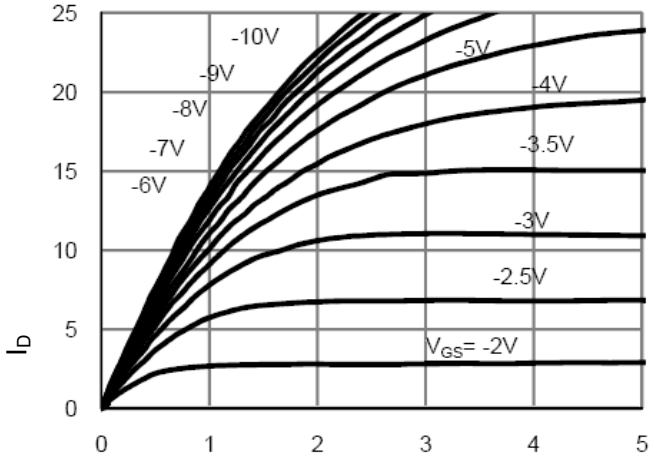



**Figure 5 Output Characteristics**

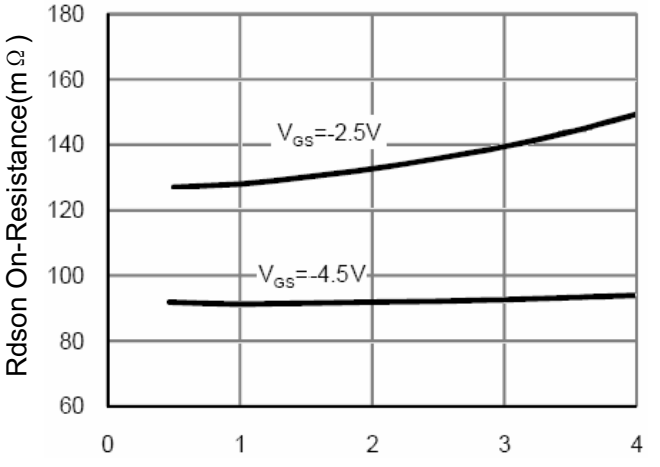



**Figure 6 Drain-Source On-Resistance**

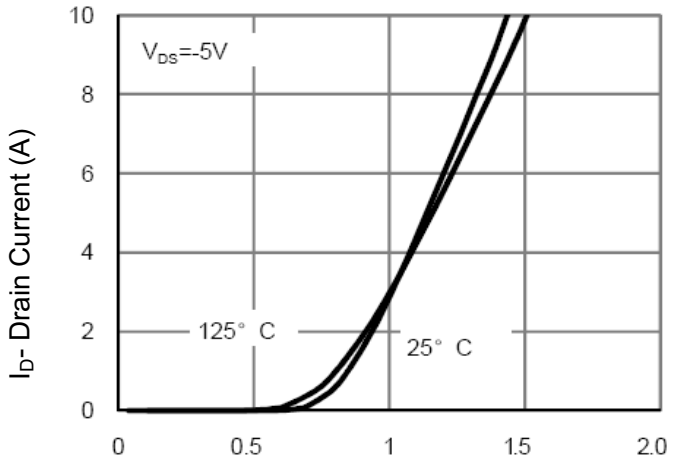



**Figure 7 Transfer Characteristics**

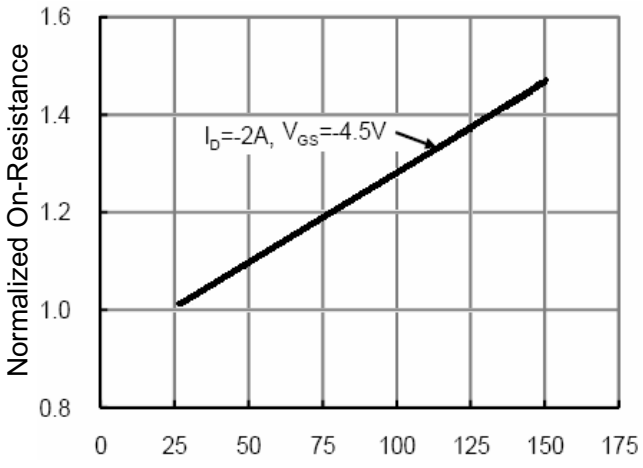



**Figure 8 Drain-Source On-Resistance**

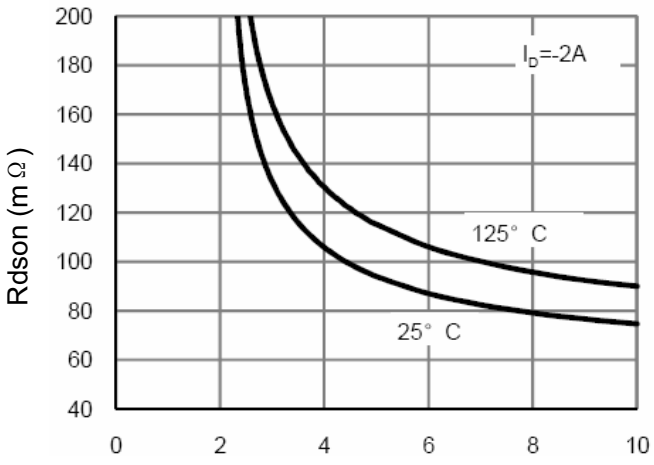



**Figure 9 Rdson vs Vgs**

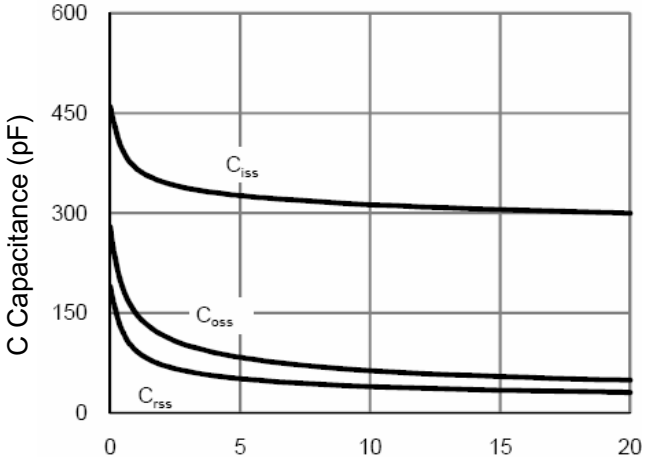



**Figure 10 Capacitance vs Vds**

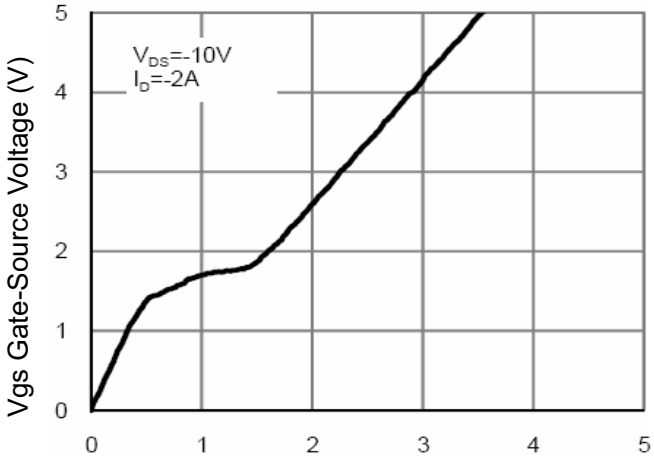



**Figure 11 Gate Charge**

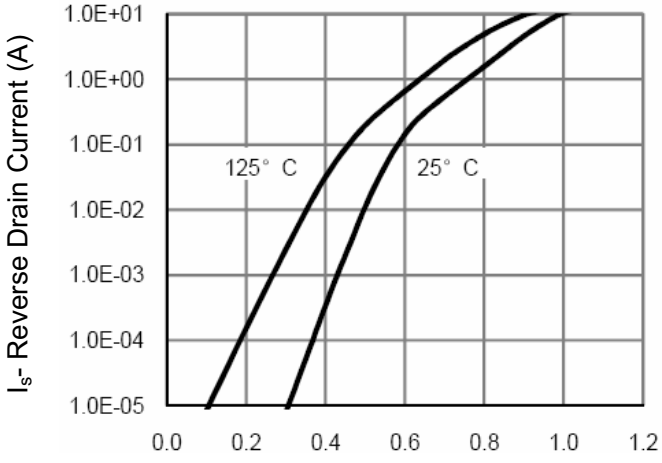



**Figure 12 Source- Drain Diode Forward**

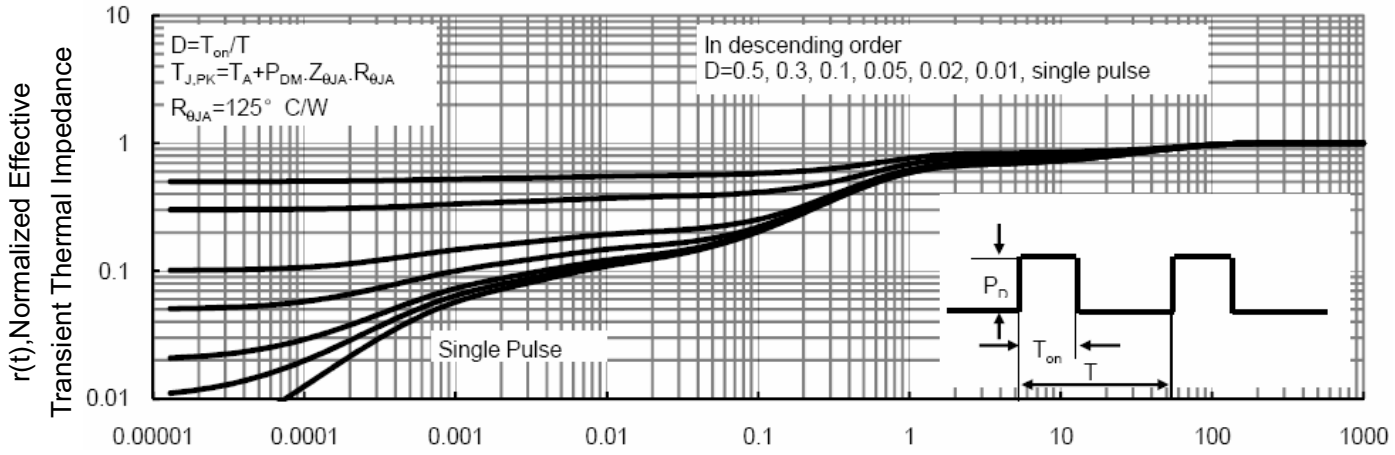
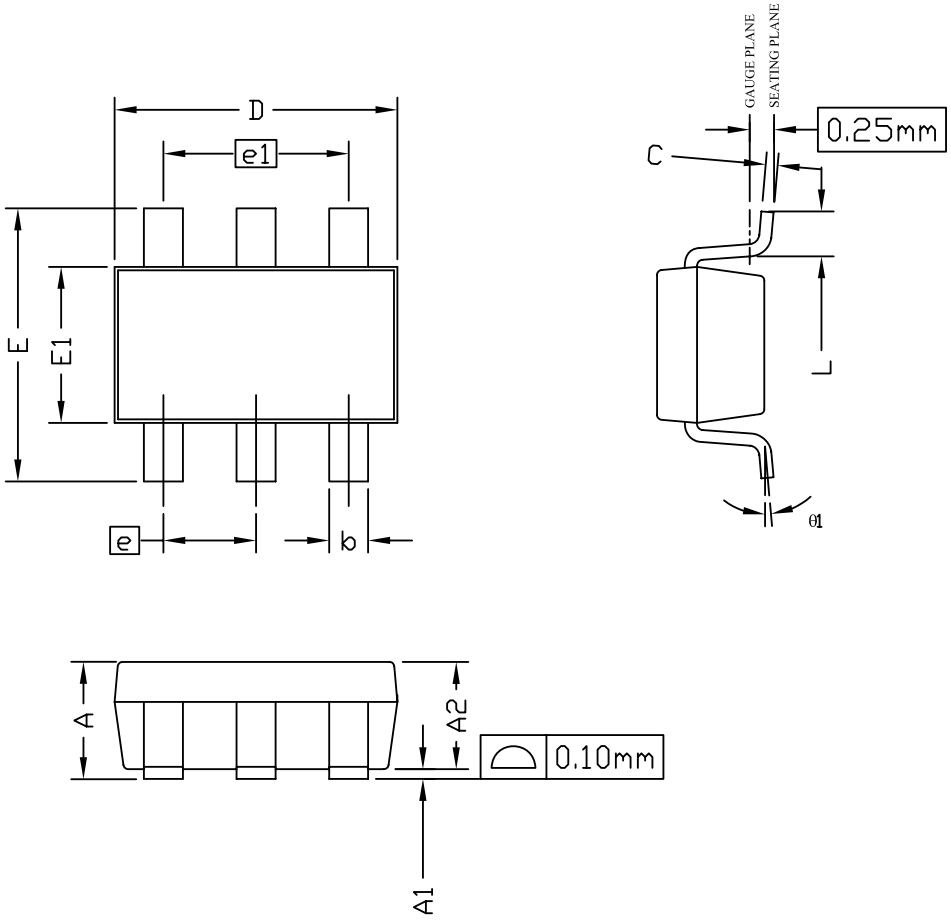


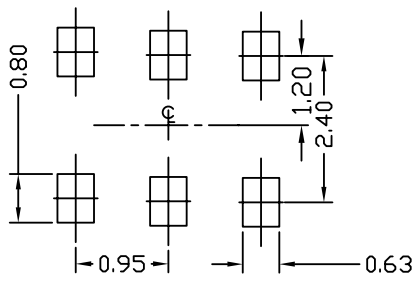

**Figure 13 Normalized Maximum Transient Thermal Impedance**

| Document No. | P0-00050 |
|---|---|
| Version | rev B |

# SOT23_6 PACKAGE OUTLINE




RECOMMENDED LAND PATTERN




| SYMBOLS | DIMENSIONS IN MILLIMETERS | | | DIMENSIONS IN INCHES | | |
|---|---|---|---|---|---|---|
| | MIN | NOM | MAX | MIN | NOM | MAX |
| A | 0.90 | --- | 1.25 | 0.035 | --- | 0.049 |
| A1 | 0.00 | --- | 0.15 | 0.00 | --- | 0.006 |
| A2 | 0.70 | 1.10 | 1.20 | 0.028 | 0.043 | 0.047 |
| b | 0.30 | 0.40 | 0.50 | 0.012 | 0.016 | 0.020 |
| C | 0.08 | 0.13 | 0.20 | 0.003 | 0.005 | 0.008 |
| D | 2.70 | 2.90 | 3.10 | 0.106 | 0.114 | 0.122 |
| E | 2.50 | 2.80 | 3.10 | 0.098 | 0.110 | 0.122 |
| E1 | 1.50 | 1.60 | 1.70 | 0.059 | 0.063 | 0.067 |
| e | 0.95 BSC. | | | 0.037BSC. | | |
| e1 | 1.90 BSC. | | | 0.075 BSC. | | |
| L | 0.30 | --- | 0.60 | 0.012 | --- | 0.024 |
| θ1 | 0° | --- | 8° | 0° | --- | 8° |

UNIT: mm

NOTE
1. PACKAGE BODY SIZES EXCLUDE MOLD FLASH AND GATE BURRS.
   MOLD FLASH AT THE NON-LEAD SIDES SHOULD BE LESS THAN 5 MILS EACH.
2. DIMENSION "L" IS MEASURED IN GAGE PLANE.
3. TOLERANCE ±0.100 mm(4 mil) UNLESS OTHERWISE SPECIFIED.
4. FOLLOWED FROM JEDEC MO-178C & MO-193C.
5. CONTROLLING DIMENSIONS IS MILLIMETER.
   CONVERTED INCH DIMENSIONS ARE NOT NECESSARILY EXACT.

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